Vincent Tong
Senior Vice President
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All Programmable 3D IC Integration:
*Leaping a Generation Ahead of Moore’s Law*
Driver #1: Insatiable Intelligent Bandwidth

What Happens in an Internet Minute?

- 639,800 GB of global IP data transferred
- 20 new victims of identity theft
- 204 million emails sent
- 47,000 app downloads
- 83,000 in sales
- 61,141 hours of music
- 20 million photo views
- 320+ new Twitter accounts
- 3,000 photo uploads
- 100,000 new tweets
- 135 new mobile users
- 100+ new LinkedIn accounts
- 6 botnet infections
- 277,000 logins
- 6 million Facebook views
- 2+ million search queries
- 30 hours of video uploaded
- 1.3 million video views

And Future Growth is Staggering

Today, the number of networked devices = the global population
By 2015, the number of networked devices = 2x the global population
In 2015, it would take you 5 years to view all video crossing IP networks each second
Driver #2: Limitations of IC Technologies

Technology: Cost, IO

- Growing gap between number of logic gates and I/O
  - 15x drop in I/O-to-logic ratio by 2020

Source: ITRS

Technology: Power

- **Power density**: primary limiting factor
- **SoCs and platforms**: demand highest performance/watt
What Does 3D Buy Us?

- Bandwidth/Watt
- Cost/Gate
- Lower Power
- Heterogeneous Integration
The First 3D FPGA

ASMBL-optimized FPGA slice

FPGA Slices Side-by-Side
Segmented Routing
High Yields Early

Silicon Interposer:
> 10K routing connections between slices
~ 1ns latency
3D Structure of a 6.8B 28nm Transistor FPGA

Microbumps
- Access to power / ground / IOs
- Access to logic regions

Through-silicon Vias (TSV)
- Bridge power / ground / IOs to C4 bumps
- Coarse pitch, low density aids manufacturability
- Etch process (not laser drilled)

Passive Silicon Interposer (65nm Generation)
- 4 conventional metal layers connect micro bumps & TSVs
- No transistors means low risk and no TSV induced performance degradation

Slide-by-Slide Die Layout
- Minimal heat flux issues
- Minimal design tool flow impact

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28nm FPGA Slice | 28nm FPGA Slice | 28nm FPGA Slice | 28nm FPGA Slice

Microbumps
Silicon Interposer
Through-Silicon Vias (TSV)
C4 Bumps
BGA Balls

Package Substrate
Advantages vs. Large Monolithic FPGAs
Capacity and Bandwidth and Power

1 Virtex-7 2000T 112 Watts
19 Watts

= 2 Largest Monolithic FPGAs
980K Monolithic FPGA
20W
980K Monolithic FPGA
20W

980K Monolithic FPGA
8W
980K Monolithic FPGA
8W

No Equivalent
Value of 3D: Bandwidth/Watt

100x bandwidth/watt advantage over conventional methods
Lower Cost Structure: Monolithic vs. Multi-Die

“Moore’s Law is really about economics” ~ Gordon Moore

<table>
<thead>
<tr>
<th>Die Area</th>
<th>Total Die Cost</th>
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<tbody>
<tr>
<td>Monolithic</td>
<td>High</td>
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<tr>
<td>Multi-Die</td>
<td>Low</td>
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The First Heterogeneous 3D FPGA

Enabling breakthrough integration for Nx100G and 400G line-card solutions

Monolithic Device

First 3D FPGA
Based on Stacked Silicon Interconnect

First Heterogeneous 3D FPGA
Based on Stacked Silicon Interconnect

Virtex-7 HT FPGAs

- Deliver leadership bandwidth, power efficiency and signal integrity
- Provide the highest number (16) of 28 Gbps transceivers – 4x the competition
- Enable build-out of economical Nx100G & 400G line cards using CFP2 optical modules
Dual FPGA Slice with 8x28Gb/s SerDes Die
All Programmable 3D IC Case Study:
Dual 100G Gearbox for CFP2 Optics

Design Challenge
- Decrease 100G port cost on communication line cards
- Decrease power consumption of 100G line cards to meet system power constraints

Solution
- Reduce **6 chip solution to one** Virtex-7 HT580T

Results
- Complete integration of the Dual Gearbox IP along with the OTN transponder IP to support **200G data throughput**
- **8 data lanes achieving 28G performance**
- Full support for the CFP2 optics requirements
- **<30 watts power** consumption
2nd Generation 3D IC (with 20nm)
Co-optimized for Extra Performance, Power, Integration

- Homogeneous/heterogeneous 3D
  - 3rd Generation fabric & die architecture
  - Wide memory for high performance buffering

- 2nd Generation 3D IC Interconnect
  - More than 5x die-to-die interconnect bandwidth
  - Industry standards interface

- Cutting Edge Functionality
  - Future XCVR protocol support (56Gb/s)

- 1.5x Integration/BOM
  - 1.5x Logic (3-4x vs. 28nm monolithic)
3D IC Supply Chain Today

FPGA, Interposer, & Package Design

28nm FPGA & Interposer

Package Substrate

μBump, Die separation CoWoS/CoC, & Assembly

Final Test of Packaged Part
Technical Challenges Posed by 3D

Cost
- Wafer backside processing is complicated
- “Device quality” wafers used for interposers
- KGD methodologies still emerging

Scalability
- Micro-bump scaling is limited
- Super-sized interposers (>30mm x 30mm)
- Improve TSV aspect ratio

Design Support
- Multi-die analysis without Multi-mode Multi-corner explosion
- Thermal modeling based on vertical hotspots
Summary

- Economic and technology forces are aligned to enable 3D stacking

- The “end game” will see three distinct technologies: Logic, Memory, Analog

- Heterogeneous integration is here!