3D ICs: Recent Advances in the Industry

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Outline

• 3D IC Background
• 3D IC Technology Development
• Summary
• Acknowledgements

Stacked Silicon Interconnect Technology Refers to Xilinx 3D solutions
3D IC Background
Technical Challenges & Costs Are Growing

- Process Technology Path Below 7nm is unclear
- Cost Reduction Slowing from Complexity / Investment Increases
- Cost Per Wafer & Cost Per Gate Deviating from Historical Reduction
Technical Challenges & Costs Are Growing

- Process Technology Path Below 7nm is unclear
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- Cost Per Wafer & Cost Per Gate Deviating from Historical Reduction

- Silicon lattice is ~ 0.5 ± 0.1 nm per 10 layers
- Our visibility always ~10 yrs - need broad exploration

IBM Systems and Technology Group

- Process Complexity has increased node to Node (This is not atypical)
- But ....
- Technical barriers have precluded new Lithographic solutions such as EUV
- This leads to extremely complex patterning solutions
- Net: neither per wafer nor per gate showing historical cost reduction trends
3DIC Extends Moore’s Law

Cost Comparison: Monolithic vs. Multi-Die

“Moore’s Law is Really About Economics”  – Gordon Moore
2.5D Technology Platform

Xilinx focus is lower CoO with 65nm DR

2.5D Si interposer
W/S<1/1um, ML>3

FPGA die partition

GPU, CPU + Memory
FPGA + ASIC

Grey Zone: Limited scalability
(multi-die integration & fine line & metal layer)

- EMIB
- Fan-out
- POSSUM
- Organic interposer
- Glass interposer

Application Processor
Baseband

AP + WIO
CPU + DRAM

AP/BB die partition

Standard fan-out
W/S<10/10um, ML<2

Advanced fan-out
W/S<3/3um, ML<3

High

I/O density

>10^4

10^3

10^2

Total silicon die area (mm^2)

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Supply Chain

- TSMC CoWoS in production
- UMC/SPIL technology is ready

TSMC CoWoS™
UMC
SPIL

Final Test & Shipment

*Re-usable cavity wafer
Xilinx 28nm 3D IC – Huge Leap in Innovation

Earth
Area: ~500 Million km²
Population: ~6.8 Billion People
Oceans: 5

Virtex-7 2000T
Interposer Area: ~775 mm²
Population: ~6.8 Billion Transistors
Chips: 5

➤ 136 Patents Awarded Worldwide
➤ 226 Pending Applications Worldwide

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3D IC Technology Development
3D IC Anatomy & Assembly Flow

Passive Silicon Interposer (65nm)
- 4 Metal Layers Connecting Micro-Bumps & TSVs

Micro-Bumps
- Power / Ground / IOs / Routing

C4 Bumps
- Connects Silicon to Package

Through-Silicon Via (TSVs)
- Connects Power / Ground / IOs to C4 Bumps

Primary Chip on Wafer Assembly Steps

- Die Attach
- Encapsulation
- Carrier Bonding
- TSV reveal
- Bump formation

> 150,000 Micro-bumps
> 10,000 TSVs
> 10,000 C4 Bumps
> 90 Processing Steps in 3D IC Flow (From Bump to Completed Package)

Package Substrate

Achieved Good Yield & Quality

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Critical Challenge: Warpage Control

- **CoWoS Technology**
  - Top dies are attached to full-thickness interposer wafers thus getting around the thin interposer warpage and poor micro-bump joining problem

- **Reconfigurable CoW (rCoW) Technology**
  - Xilinx patent issued worldwide (US/TWN/CN/EU/IND/JPN/KR)
  - Release layer approach that withstands reflow & maintains low warpage

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**Key 1.** Coat the proprietary release layer (Reflowable/detachable)

**Key 2.** Reconfigures & flattens the interposers (<10um) on cavity wafer

**Key 3.** Carry out wafer-scale clean & u-scale defect mapping

**Key 4.** Enable top die standard reflow & deflux (instead of special T/C bond)

**Key 5.** Simple mechanical detach from carrier

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**Warpage control**

Keep warpage below <10um over entire temp range

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HTS Aging Reliability Issue

- Voiding or crack in micro-joint during long term stress (HTS in particular)
  - Due to limited Sn source and its dual consumption rate from top and bottom pad
- Resolution: Heavy Cu doping into LF solder cap (with Ni barrier layer)
  - Take advantages of ductile IMC (Cu-Sn) and slower IMC reaction (Ni with Cu-Sn IMC)
  - Passed 3X reflow + 150°C aging condition for > 1000 hrs

Diffusion flux model of inter-diffusion

HTS aging performance

- Fast Cu-Sn reaction
- Kirkendal void form
- Ductile IMC
- Brittle NiSn IMC
- Slow IMC reaction
- Large Vol shrinkage
- Stable Cu-Sn IMC
- Super slow IMC reaction

*Reference images (from no-doping u-bump)
Leadership Continues at 20/16nm - UltraSCALE

- 4.4M Logic Cells in 20nm
- 14B transistors
- 600,000 micro-bumps
- 55mm package, 2892 pins
Leadership Continues at 20/16nm - UltraSCALE

- 2.0 dB insertion loss at Nyquist Frequency
- Low loss substrate and design
- 23,000 C4 bumps
Demo High Performance Mixed Signal Integration

- **2 x Virtex-7 350T slices**
- **Array of 16 DACs**
  - 16-bit – 1.6GS/s
- **Array of 16 ADCs**
  - 13-bit – 125MS/s

➤ **Industry first 3D FPGA/Mixed Signal integration (ISSCC 2014)**
Si-Less/TSV-less Interconnect Tech (SLIT) Builds on Interposer

Key Benefits

- **Lower cost of ownership**
  - No HR-Si substrate used & less process modules (No TSV module/TBDB/TSV revealing)

<table>
<thead>
<tr>
<th>Structure</th>
<th>SLIT (Under development)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-R Si substrate</td>
<td>×</td>
</tr>
<tr>
<td>65nm 4X Metal</td>
<td>○</td>
</tr>
<tr>
<td>TSV Creation</td>
<td>×</td>
</tr>
<tr>
<td>Micro-bumping</td>
<td>○</td>
</tr>
<tr>
<td>Temporary carrier</td>
<td>○</td>
</tr>
<tr>
<td>Thinning</td>
<td>□</td>
</tr>
<tr>
<td>TSV Revealing</td>
<td>×</td>
</tr>
</tbody>
</table>

Xilinx, SPIEL (iMAPS 2014)
## 3D IC Technology Landscape

<table>
<thead>
<tr>
<th>Players</th>
<th>Chip level</th>
<th>Device level</th>
<th>W2W C2W level</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Samsung</strong> DRAM / <strong>Hynix</strong> NAND &amp; DRAM / <strong>IBM</strong> / <strong>Micron</strong> / <strong>Elpida</strong> / <strong>Qualcomm</strong> / <strong>Nokia</strong></td>
<td><strong>Samsung</strong> Vertical-Gate NAND/ <strong>Besang</strong> / Monolithic 3D IC / Stanford</td>
<td><strong>SONY (Stacked CIS)</strong> / <strong>Tezzaron</strong> / Ziptronix/ MIT Lincon Lab</td>
</tr>
<tr>
<td>TSV size</td>
<td>5~10um</td>
<td>0.5~2um contact through oxide</td>
<td>2~5um in diameter</td>
</tr>
<tr>
<td>TSV pitch</td>
<td>30~50um</td>
<td>1~4um (not limited)</td>
<td>5~10um</td>
</tr>
<tr>
<td>TSV count</td>
<td>1k~5k</td>
<td>Not limited</td>
<td>Not limited</td>
</tr>
</tbody>
</table>

### Key features

- **Samsung**: 16Gb DRAM 9MCP (2110)
- **Hynix**: DRAM Stack
- **Micron HMC**: Cross-sectional structure
- **Elpida**: Cu TSV & Bump
- **Nokia**: Interface Die
- **Tezzaron**: Oxide-to-oxide bond
- **Ziptronix**: Cu-to-Cu bond
- **Besang**: Vertical gate

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Summary

- Economic and technology forces are aligned to enable 2.5D/3D stacking

- TSV and 3D stacking already deployed in Smartphones, High end FPGAs & Servers

- The “end game” will see three distinct technologies: Logic, Memory, Analog
Acknowledgements

• Xilinx
  - R&D, Reliability, NPI, Operations and Marketing Teams

• Partners
  - TSMC R&D and Production Teams for FPGA, CoWoS
  - UMC for Interposer
  - SPIL R&D for MEOL and Advanced Packaging
  - Fujitsu Interconnect Technology for High Speed Substrates
## Design Rule Comparison

<table>
<thead>
<tr>
<th>Design Rules for Die to Die Interconnection</th>
<th>MCM (Substrate)</th>
<th>EMIB</th>
<th>Silicon Interposer (65 nm BEOL)</th>
<th>WLFO / Organic Interposer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Bump pitch (um)</td>
<td>150 (C4)</td>
<td>150 (C4)</td>
<td>40 (u-bump) bridge</td>
<td>&lt; 40 (u-bump)</td>
</tr>
<tr>
<td>Via size / pad size (um)</td>
<td>60 / 90</td>
<td>0.4 / 0.7</td>
<td>0.4 / 0.7</td>
<td>10/30</td>
</tr>
<tr>
<td>Minimum Line &amp; Space (um)</td>
<td>15 / 15</td>
<td>0.4 / 0.4</td>
<td>0.4 / 0.4</td>
<td>3 / 3</td>
</tr>
<tr>
<td>Metal thickness (um)</td>
<td>10</td>
<td>1</td>
<td>1</td>
<td>2-5</td>
</tr>
<tr>
<td>Dielectric thickness (um)</td>
<td>30</td>
<td>1</td>
<td>1</td>
<td>&lt; 5</td>
</tr>
<tr>
<td># of die-to-die connections per layer + GND shield layer (2L)</td>
<td>100’s</td>
<td>10,000’s</td>
<td>10,000’s</td>
<td>1000’s</td>
</tr>
<tr>
<td>Minimum die to die spacing (um)</td>
<td>4000</td>
<td>Bridge ~ 2500</td>
<td>150</td>
<td>&lt; 250</td>
</tr>
<tr>
<td># of High density layers feasible</td>
<td>Not a limitation</td>
<td>Not a limitation</td>
<td>Not a limitation</td>
<td>1-3L layers</td>
</tr>
<tr>
<td>Die Sizes for assembly and # of assemblies</td>
<td>Not a concern</td>
<td>Size &amp; # limitation?</td>
<td>Not a concern</td>
<td>Size limitation?</td>
</tr>
</tbody>
</table>

Xilinx pursuing Silicon Interposer for design rule density, BW and lower power – e.g. die partition

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